Proposal for a Semester’s Thesis at the Institute of Robotic and Embedded system

Time-triggered OS (TT-OS) Development

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Project Description

In the context of TU9 project, research at the Institute of Robotics and Embedded Systems is dealing with the challenge of providing high-performance ECUs as an enabling technology applicable in the automotive field, which will enable a simple centralized multi-core system. The transition from single-core to multi-core brings several benefits on the component level of the E/E architectures, such as (1) improving the performance per watt and enabling higher levels of parallelism; (2) the reduction of wiring costs and mounting efforts (3) the gain in flexibility and reliability [1]. Regarding electric vehicle, a fully deterministic real-time behavior should be guaranteed. Time-triggered execution models can offer a fully deterministic real-time behavior for safety-critical systems. Current practice in many safety-critical system domains, such as electric vehicle [2] and avionics systems [3], favors a time-triggered approach [1]. The goal of this project is to develop a time-triggered operation system (TT-OS) for our proposed platforms. TT-OS architecture need to demonstrate very low levels of task jitter, and they can maintain their low-jitter characteristics even when techniques such as dynamic voltage scaling (DVS) or cache partitioning are employed to reduce system power consumption and improve system performance. The project will include the following phases:

- Design time-triggered operation system.
- Software interface design for different hardware (Be friendly to port OS to different hardware).
- Case study: integrate dynamic voltage scaling (DVS) or cache partitioning into TT-OS

This work will be carried out in TU9 project to which the Institute of Robotics and Embedded Systems is contributing in terms of hardware and software design and performance analysis.

Kind of Work

- 30% theory
- 40% implementation
- 20% evaluation
- 10% documentation

Requirements

- good knowledge on C/C++ and Real-time OS.
- good knowledge of FPGA design flow with VHDL or Verilog HDL.
- ability to acquaint yourself with an unfamiliar software design environment.
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References

