Introduction to FPGA programming

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What is an FPGA

• FPGA: Field Programmable Gate Array
• Integrated circuit that can be reconfigured
• Logic gates on FPGA can built any kind of circuit
  – FlipFlops, DSP, Memory and even CPUs
• HDL is used for specification
  (Verilog or VHDL)
DE2-115 board

- Altera Cyclone IV EP4CE115F29C7N FPGA (114k LEs)
- USB Blaster for configuring and programming
- Green and red LEDs
- Buttons and Switches
- GPIO
- Many devices and connectors on board
Development Environment

• Altera QuartusII
  - Synthesis tool for HDL designs
  - Supports graphical hardware design
  - Includes SOPC Builder to generate Computer Systems
    • Based on NiosII CPU
    • Library of memory controllers/interfaces and peripherals
  - Includes Nios2SBT to develop software for the NiosII CPU
NiosII CPU

- 32bit RISC architecture
- 3 variants: economy, standard, fast
- JTAG support
- Support up to 2GB of memory
- Soft-core, can be configured with:
  - Cache, branch prediction, pipelining, ...
QuartusII Editions

- Subscription Edition (paid)
- Web Edition (free)
  - Includes all features of Subscription Edition
  - Some Components (advanced NiosII CPUs or Ethernet) need a separate licence (hardware must be connected to Quartus)
  - Simple NiosII CPU (NiosII/e) free for unlimited use
How to generate a System (summary)

- Generate a Block Diagram file
- Generate SOPC system
- Instantiate SOPC system in block diagram
- Add wires and pins
- Compile and program FPGA

- Detailed howtos: check course homepage
Programming the FPGA

- In JTAG mode: set SW19 to RUN
  - Download .sof file to FPGA using Quartus II Programmer
  - FPGA loses configuration with every reset
- In AS (Active Serial) mode: set SW19 to PROG
  - Download .pof file to EPCS64 using Quartus II Programmer
  - Set SW19 to RUN and reboot the device
  - FPGA is re-programmed with every reset
The Nios2SBT IDE

- Generate software for the NiosII CPU
- Board Support Package (BSP) for hardware abstraction
- Application project uses BSP
- Stdout is sent through JTAG UART and shown in Nios2SBT
Exercise

- Generate a basic FPGA configuration including:
  - NiosII CPU
  - On-chip memory
  - JTAG-Uart
  - Timer

- Verify correctness by printing „Hello World“