Master Thesis Proposal
Customized FPGA Accerated Board Design with OpenCL Support

Technische Universität München

Fakultät für Informatik

Lehrstuhl für Echtzeitsysteme und Robotik

Supervisor:
Prof. Dr.-Ing Alois Knoll

Advisor:
Dr. Kai Huang
Biao Hu M.Sc.

Research project:
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Type:
BA/MA

Research area:
Machine Learning and Parallel Programming

Programming language:
OpenCL, C++

Required skills:
Good at C++, Machine Learning

Language:
englisch

Date of submission:
25. Juli 2016

For more information please contact us:

Phone: +49.89.289.18134

E-Mail: huangk@tum.de
hub@in.tum.de

Internet: www6.in.tum.de

Background

In the context of TU9 project, research at the Institute of Robotics and Embedded Systems is dealing with the challenge of providing high-performance ECUs as an enabling technology applicable in the automotive field, which will be a heterogeneous system with multi-core CPU, FPGA, and GPU.

Open Computing Language (OpenCL) provides us a great chance to make the heterogeneous system work harmoniously. OpenCL is a framework for writing programs that execute across heterogeneous platforms consisting of central processing units (CPUs), graphics processing units (GPUs), digital signal processors (DSPs), field-programmable gate arrays (FPGAs) and other processors or hardware accelerators. OpenCL specifies a programming language (based on C99) for programming these devices and application programming interfaces (APIs) to control the platform and execute programs on the compute devices. OpenCL provides a standard interface for parallel computing using task-based and data-based parallelism.

Motivation and Goals

Although OpenCL provides us the capability to access all processing units in a same program, we are limited to use the processor products that were given OpenCL board support package to support OpenCL programming. It was impossible for us to design our own board to run OpenCL program. However, it now seems possible to design our FPGA board to run OpenCL program as the FPGA producer-Altera company has released the OpenCL Custom Platform Toolkit nowadays.

The motivation of designing a new FPGA board to run OpenCL program, instead of buying a on-the-shelf product, is that the customized FPGA will be specialized to be more effective in accelerating some advanced driving assistant systems (ADASs). In order to achieve this, we would need to design a new board with an Intel CPU as a host as well as a powerful Altera stratix chip as an accelerator, where Intel CPU and FPGA chip communicate by PCIe bus.

Tasks

- Design a PCB with Stratix FPFA, compliant with the Altera OpenCL interface[1].
- Build the Board Support Package (BSP) that enables the software toochain for this customized PCB.
- Test our available ADAS applications on this PCB.

Research Area

High performance embedded computing

Required Skills

PCB design, FPGA

[1] https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/opencl-sdk/ug_aocl_custom_platform_toolkit.pdf