Embedded Cortical Learning with Hierarchical Temporal Memory

BACKGROUND
Hierarchical Temporal Memory (HTM) [1] is a computational model of information processing in the neocortex of mammalian brains. Although based on a network of neurons which are interconnected by synapses, the HTM model is completely different from standard artificial neural networks. It is designed for processing time-varying data streams and therefore especially interesting for applications in robotics and neurorobotics [2]. Possible prospective applications are – among many others – model learning and error detection. However, in most robots, both space and energy are highly limited, which makes an efficient embedded implementation of the HTM algorithms an inevitable requirement for a future use in robotics.

YOUR TASK
The Parallella Board [3] is a both small and power-efficient system with an on-board multicore chip based on the Epiphany architecture. In this project, you will develop an efficient parallel implementation of the HTM model which is optimized for Epiphany. Using appropriate benchmark tasks, you will then analyze how the performance and the power consumption of your implementation compare to the reference code running on a standard CPU core.

REQUIRED SKILLS
- Good knowledge of C/C++
- Experience in parallel programming
- Basic knowledge about microprocessor architectures

FURTHER READING

CONTACT
Florian Walter
florian.walter@tum.de