Master’s Thesis: VHDL FPGA implementation of cache architecture and its benchmarking and testing

In PAR group we are researching on novel software and hardware chip multi processor (CMP) architectures suitable for various applications. For example, applications like multimedia need very high performance while safety critical applications need timing guarantees. Caches improve performance of an architecture by reducing memory access latencies. But, their timing behavior is highly unpredictable; the access latency difference between a cache hit and a cache miss can be in order of 100x clock cycles in modern processors. In Chip Multi Processors (CMP) the penalty of a cache miss is even larger due to congestion on the main memory. In Hard Real Time (HRT) applications, deadlines are in terms of microseconds or less. In such applications missing a deadline once (may be due to a cache miss) can endanger lives (e.g. Safety Critical Applications). Thus, a predictable cache architecture is necessary whose timing behavior is known statically to guarantee that dead lines will be satisfied.

The main goal of the thesis is to implement a cache architecture whose timing behavior is predictable and its onchip resource utilization is reasonable. The thesis is comprised of, but not limited to, the following tasks:

- Analysis of various cache architectures and their suitability for different applications. Particular merits are: Timing predictability, area and operating frequency.
- Implementation of the most suitable cache architecture into Altera FPGA using VHDL.
- Building a test bench for the implementation.
- Porting benchmarks to the final architecture and comparing the results with the state-of-art architectures.
- Research value to the thesis can be added by inventing novel cache architecture suitable for safety critical applications (optional).

In our group we are using industry standard tools like Mentor Modelsim and Altera Tool chain (Quartus, NIOS IDE etc.). We also have Xilinx FPGA and tool chain facility at our group.
Prerequisites:

- FPGA development (Altera, VHDL)
- C programming language
- General Understanding of Embedded Processors and Memory hierarchy

Contact information:

- Supervisor: Prof. Dr. Alois Knoll (Robotics and Embedded Systems, Dept. for Computer Science, Technische Universität München)
- Advisors
  - Hardik Shah <shah@fortiss.org>
  - Andreas Raabe <raabe@fortiss.org>